Low Noise, Zero-Drift, Precision Operational Amplifier

Features

- **Low offset voltage: 25 μV Maximum per Amplifier**
- **Zero drift: 0.05 μV/°C**
- **Low noise: 12 nV/√Hz**
- **0.1-Hz to 10-Hz Noise: 800 nV_{PP}**
- **PSRR: 130 dB**
- **CMRR: 120 dB**
- **Open-loop gain: 140 dB**
- **Gain bandwidth: 1.5 MHz**
- **Quiescent current: 500 μA (MAX)**
- **Wide supply range: ±2 V to ±17 V**
- **Rail-to-rail output:**
  Input includes negative rail
- **RFI filtered inputs**

Applications

- **Weight scale**
- **Analog input module**
- **Flow transmitter**
- **Battery test**
- **DC power supply, ac source, electronic load**
- **Data acquisition (DAQ)**
- **Semiconductor test**

General Description

The OPA188 (single) and OPA2188 (dual) operational amplifier use proprietary auto-zeroing techniques to provide low offset voltage (25-μV maximum) and near zero-drift over time and temperature. These miniature, high-precision, low-quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 15 mV of the rails.

The input common-mode range includes the negative rail.

Either single or dual supplies can be used in the range from 4 V to 34 V (±2 V to ±17 V). The OPA188 is available in SOT23-5 packages. The OPA2188 is available in MSOP-8、SOIC-8 and TSSOP-8 packages. All versions are specified for operation from –55°C to +125°C.

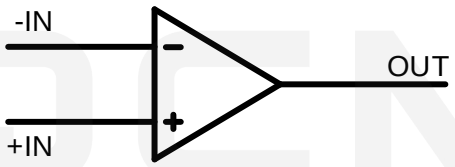


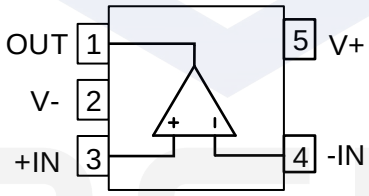
Figure 1. Simplified Schematic

Package/Order Information

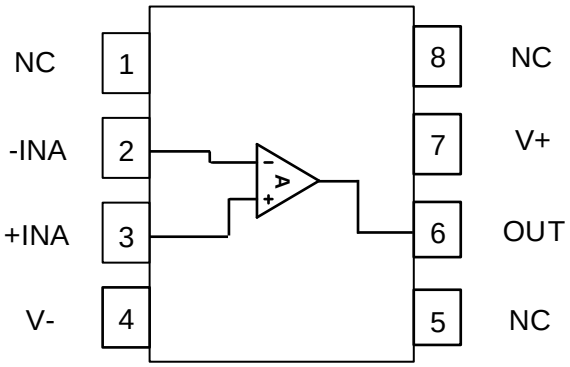
MODEL	Op Temp(°C)	ORDERING NUMBER	PACKAE DESCRIPTION
OPA188	-55°C~125°C	OPA188AIDBVR	SOT23-5
	-55°C~125°C	OPA188AIDR	SOIC-8 (SOP-8)
OPA2188	-55°C~125°C	OPA2188AIDR	SOIC-8 (SOP-8)
	-55°C~125°C	OPA2188AIDGKR	TSSOP-8

Pin Configuration and Functions (Top View)

Pin Description



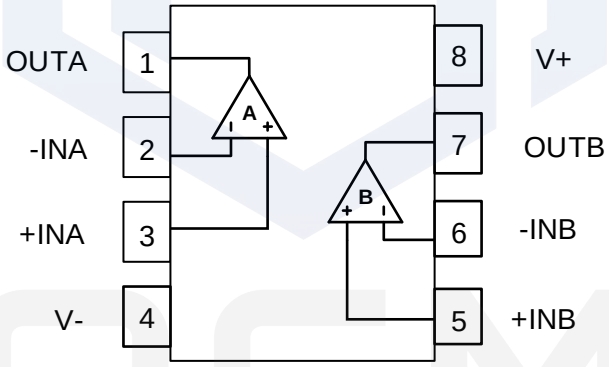
SOT23-5



SOIC-8

OPA188

PIN			I/O	DESCRIPTION
NAME	SOT	SOIC-8		
+IN	3	3	I	Positive (noninverting) input
-IN	4	2	I	Negative (inverting) input
OUT	1	6	O	Output
V+	5	7	-	Positive (highest) power supply
V-	2	4	-	Negative (lowest) power supply



SOIC-8/TSSOP8

OPA2188

PIN		I/O	DESCRIPTION
NAME			
+INA	3	I	Noninverting input, channel A
+INB	5	I	Noninverting input, channel B
-INA	2	I	Inverting input, channel A
-INB	6	I	Inverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

Specifications

Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage	Supply Voltage		±20	V
	Signal Input Terminals Voltage(2)	(V-) - 0.5	(V+) + 0.5	V
Current	Signal Input Terminals Current(2)	-10	10	mA
	Output Short-Circuit(3)	Continuous		
θ_{JA}	Operating Temperature Range	-55	125	°C
	Storage Temperature Range	-65	150	°C
	Junction Temperature		150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage，Vs= (V+) - (V-）	Single-supply	±2	±17	V
	Dual-supply	4	34	V

Electrical Characteristics

At T_A = 25°C, V_S = ±15V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input Offset Voltage			7.5	25	µV
dV_{OS}/dT	Input Offset Voltage Average Drift	T_A = -55°C to 125°C		0.05		µV/°C
INPUT CURRENT						
I_B	Input Bias Current			50		pA
I_{OS}	Input Offset Current			100		pA
NOISE						
V_N	Input Voltage Noise	f=0.1Hz to 10Hz		800		nV_{PP}
e_N	Input Voltage Noise Density	f= 1kHz		12		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-Mode Voltage Range		V-		(V+)-1.5	V
CMRR	Common-Mode Rejection Ratio	(V-)+1.5 ＜VCM＜ (V+)-1.5		120		dB
FREQUENCY RESPONSE						
GBW	Gain-Bandwidth Product			1.5		MHz
SR	Slew Rate	G = +1		1.5		V/µs
Ts	Settling Time			1		µs
OUTPUT						
A_V	Open-Loop Voltage Gain			140		dB
$V_{OUT-SWING}$	Output Swing from Rail	No load		5	15	mV
POWER SUPPLY						
PSRR	Power-Supply Rejection Ratio			130		dB
V_S	Operating Voltage Range	I_O=0A	4		34	V
I_Q	Quiescent Current/Amplifier	I_O=0A		304	500	µA

Typical Characteristics

At T_A = 25°C, V_S = ±15V, V_{CM}= V_S /2, R_L=10kΩ unless otherwise noted.

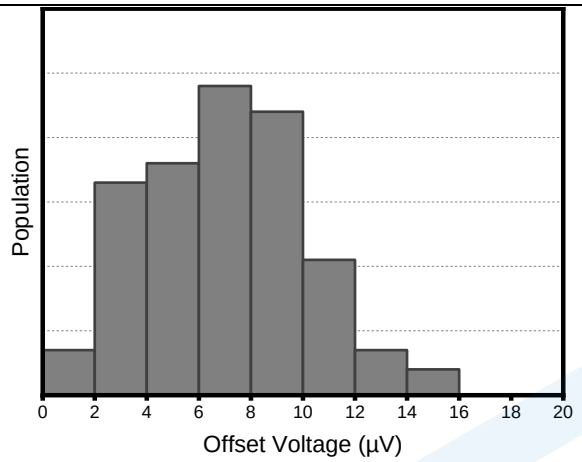


Figure 2. Offset Voltage Production Distribution

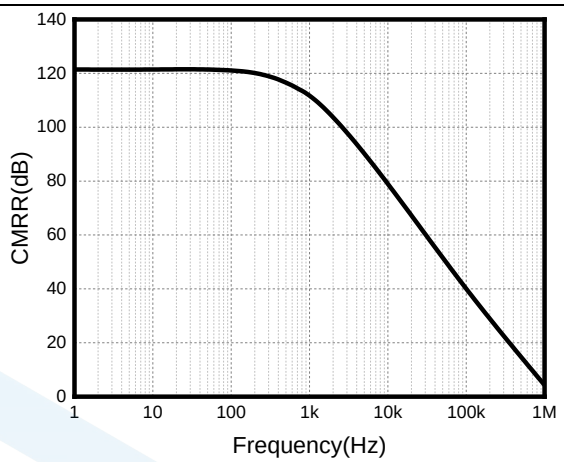


Figure 3. CMRR vs Frequency

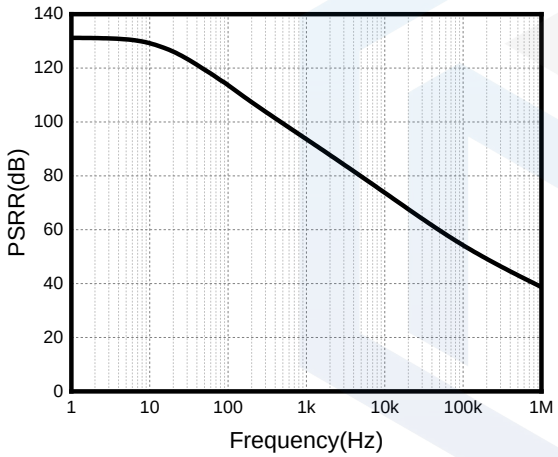


Figure 4. PSRR vs Frequency

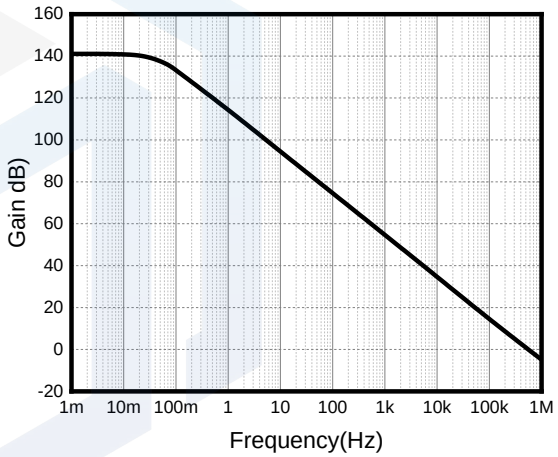


Figure 5. Open-Loop Gain vs Frequency

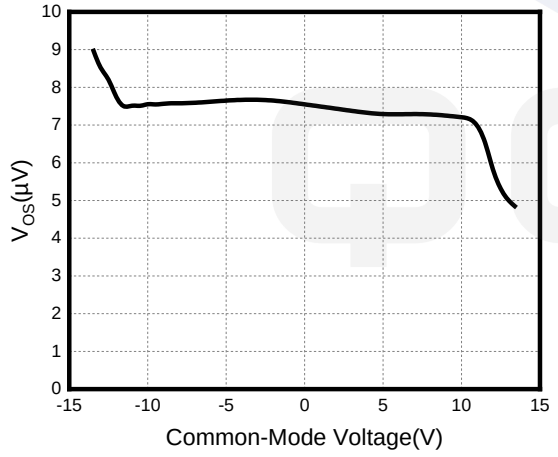


Figure 6. Offset Voltage vs Common-Mode Voltage

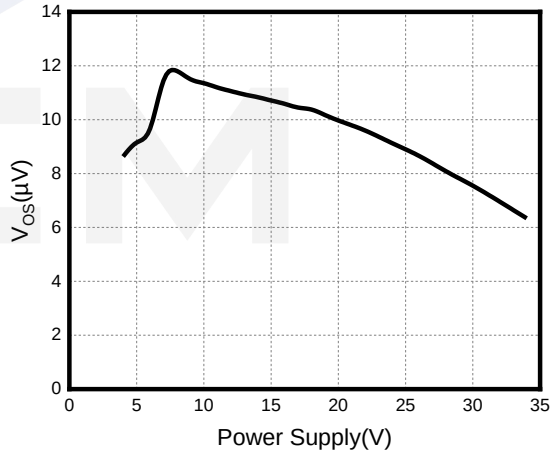


Figure 7. Offset Voltage vs Power Supply

Typical Characteristics

At T_A = 25°C, V_S = ±15V, V_{CM}= V_S /2, R_L=10kΩ unless otherwise noted.

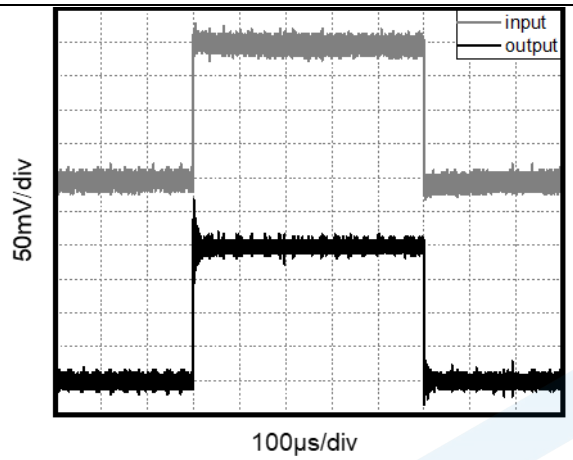


Figure 8. Small-Signal Step Response

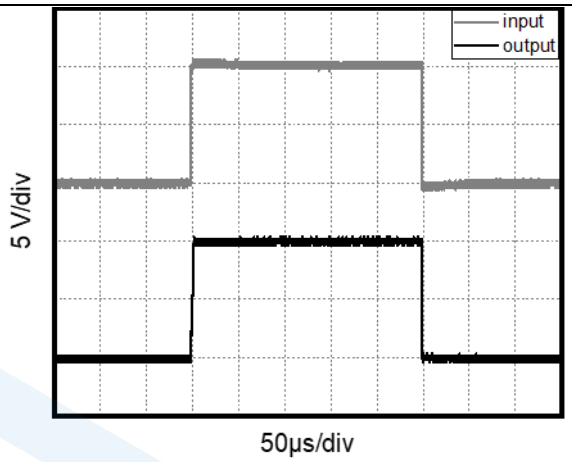


Figure 9. Large-Signal Step Response

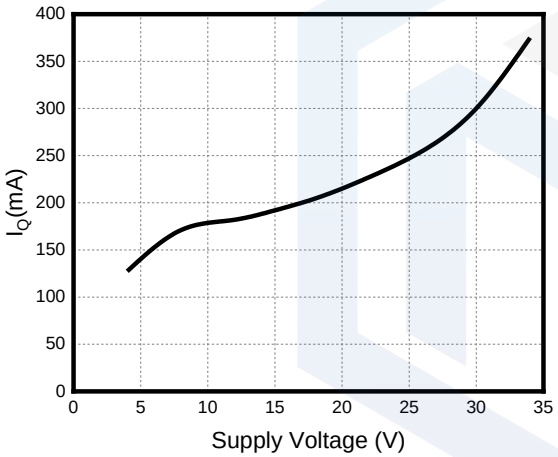


Figure 10. Quiescent Current vs Supply Voltage

Detailed Description

Overview

The OPA188/2188 operational amplifier combines precision offset and drift with excellent overall performance, making this device an excellent choice for many precision applications. The precision offset drift of only 0.05 μV/°C provides stability over the entire temperature range. In addition, this device offers excellent overall performance with high CMRR, PSRR, and AOL. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

The OPA188/2188 device is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from 4 V to 36 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultralow broadband noise and zero flicker noise.

Typical Applications

Voltage Follower

As shown in Figure 11, the voltage gain is 1. With this circuit, the output voltage V_{OUT} is configured to be equal to the input voltage V_{IN}. Due to the high input impedance and low output impedance, the circuit can also stabilize the output voltage, the output voltage expression is

$$V_{OUT}=V_{IN} \quad (1)$$

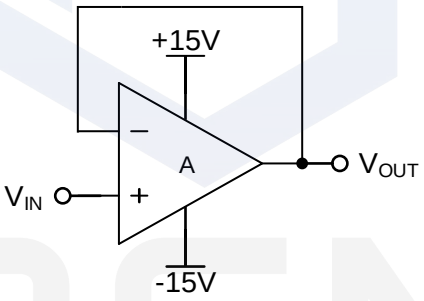


Figure 11. Voltage Follower

Inverting Proportional Amplifier

As shown in Figure 12, for a reverse-phase proportional amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R1 to R2. The output voltage V_{OUT} is inversely with the input voltage V_{IN}. The input impedance of the circuit is equal to R1, and the output voltage expression is

$$V_{OUT}=-\frac{R2}{R1}V_{IN} \quad (2)$$

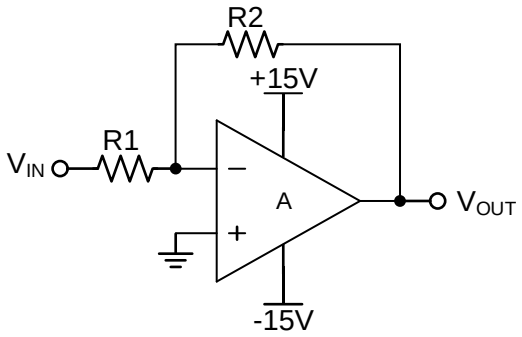


Figure 12. Inverting Proportional Amplifier

Noninverting Proportional Amplifier

As shown in Figure 13, for a noninverting amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R1 to R2. The output voltage V_{OUT} is in phase with the input voltage V_{IN}. In fact, this circuit has a high input impedance because its input side is the same as the input side of the operational amplifier. The output voltage expression is

$$V_{OUT}=(1+\frac{R2}{R1})V_{IN} \quad (3)$$

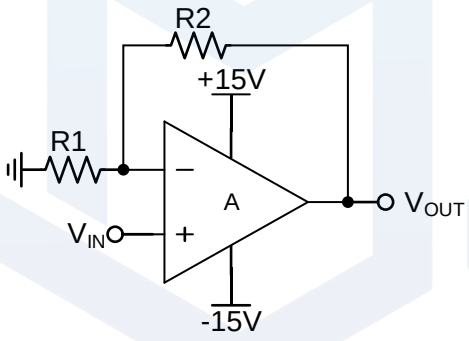


Figure 13. Noninverting Proportional Amplifier

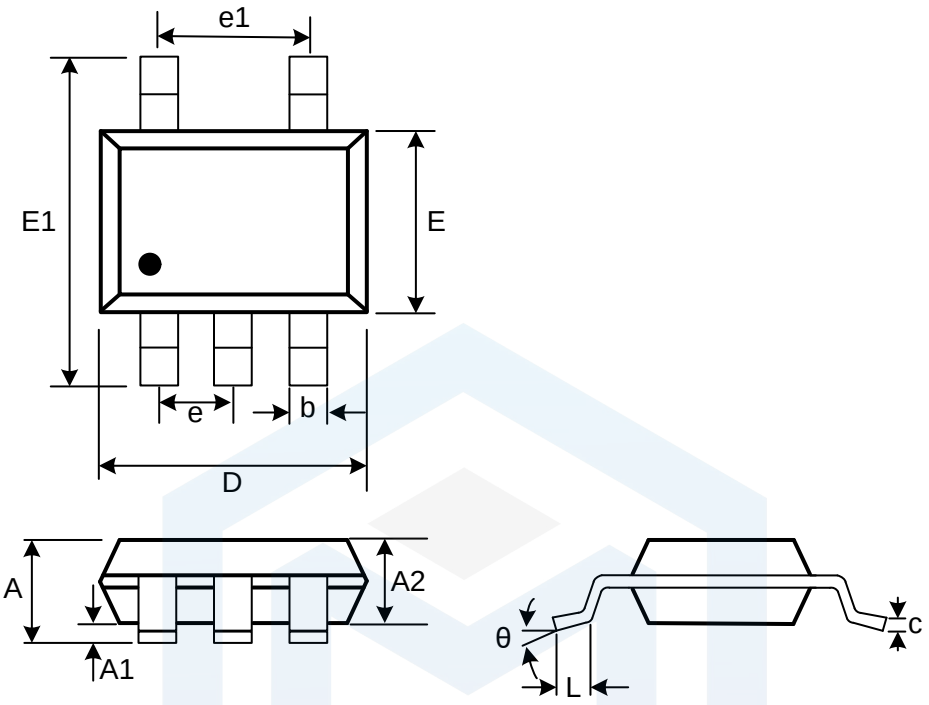
Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

Package Description

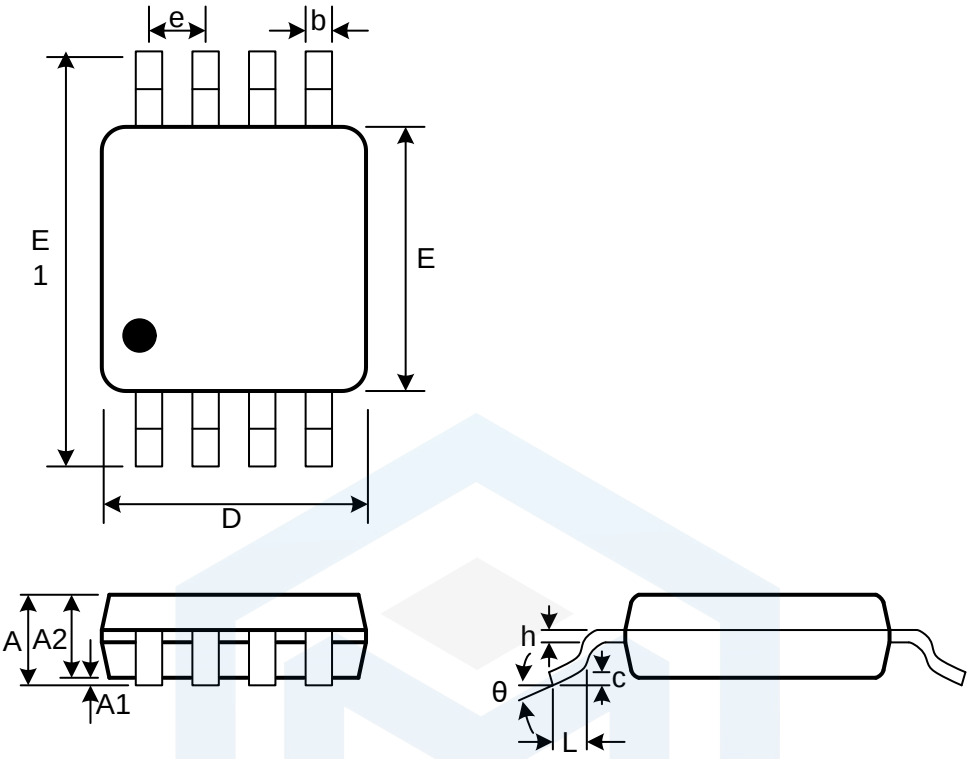
SOT23-5



(Unit: mm)

Symbol	Min	Max
A	1.05	1.25
A1	0	0.1
A2	1.05	1.15
b	0.3	0.5
c	0.1	0.2
D	2.82	3.02
e	0.95(BSC)	
e1	1.9(BSC)	
E	1.5	1.7
E1	2.65	2.95
L	0.3	0.6
θ	0°	8°

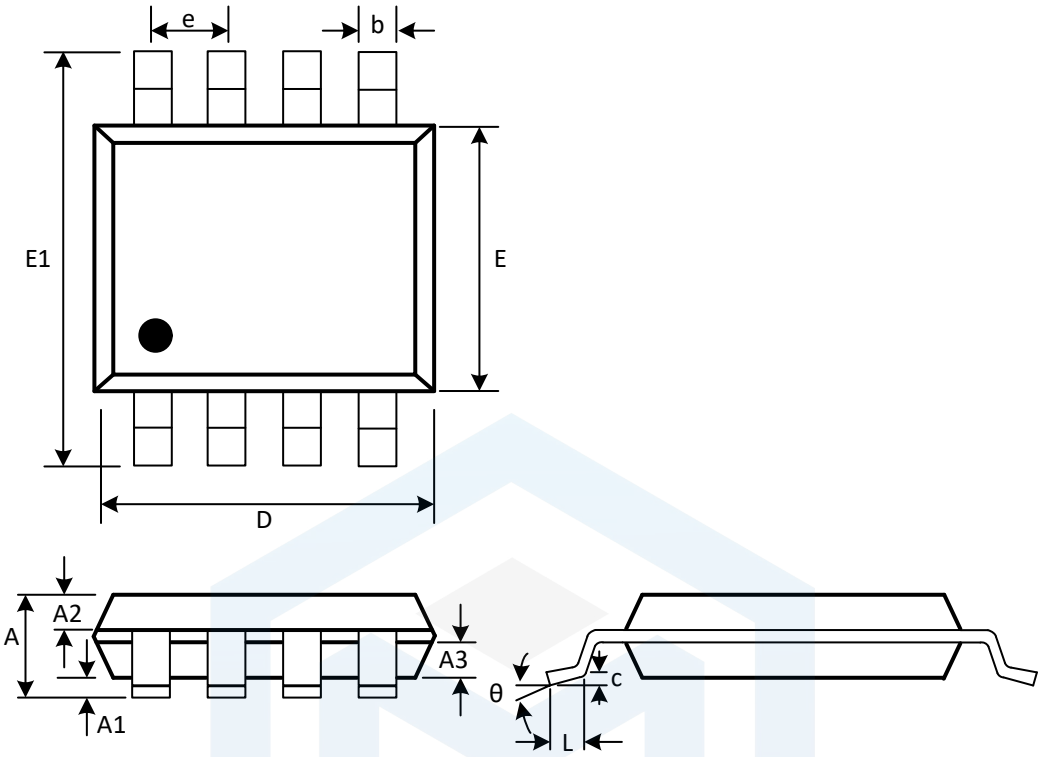
MSOP-8



(Unit: mm)

Symbol	Min	Max
A		1.100
A1	0.050	0.150
A2		0.950
b	0.250	0.380
c	0.250	
D	2.900	3.100
e	0.650(BSC)	
E	2.900	3.100
E1	4.750	5.050
h	0.130	0.230
L	0.400	0.700
θ	0°	8°

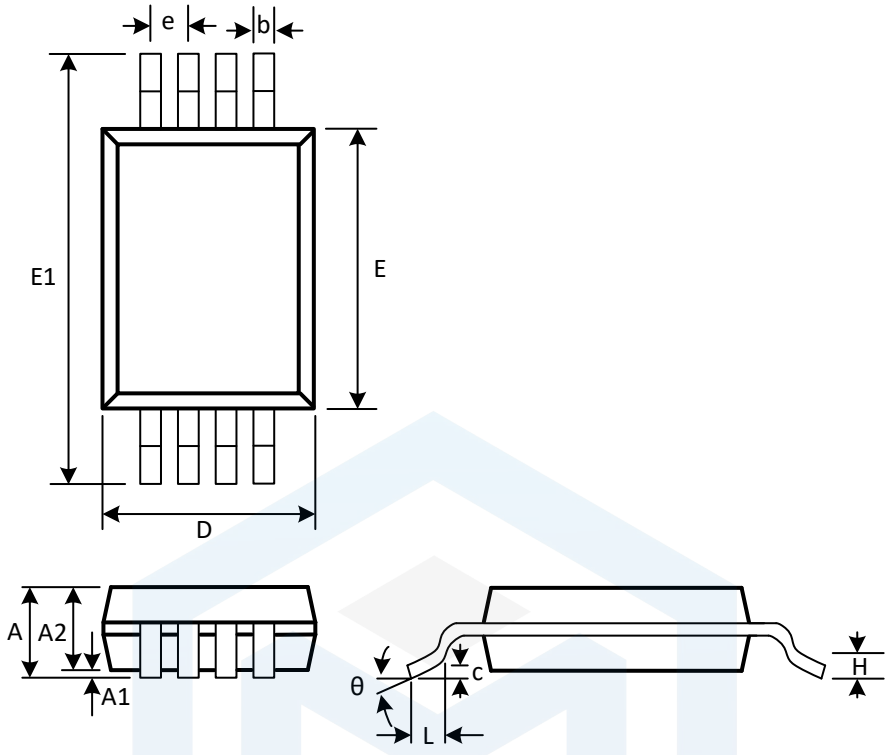
SOIC-8



(Unit: mm)

Symbol	Min	Max
A	1.300	1.600
A1	0.050	0.200
A2	0.550	0.650
A3	0.550	0.650
b	0.356	0.456
c	0.203	0.233
D	4.800	5.000
e	1.270(BSC)	
E	3.800	4.000
E1	5.800	6.200
L	0.400	0.800
θ	0°	8°

TSSOP-8



(Unit：mm)

Symbol	Min	Max
A		1.100
A1	0.050	0.150
A2	0.800	1.000
b	0.190	0.300
c	0.090	0.200
D	2.900	3.100
e	0.650(BSC)	
E	4.300	4.500
E1	6.250	6.550
H	0.250	
L	0.500	0.700
θ	1°	7°